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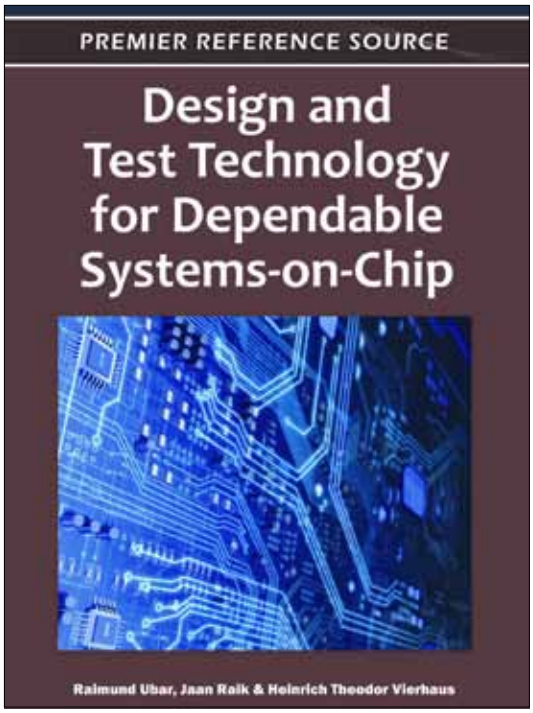
Design and Test Technology for Dependable Systems-on-Chip



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Designing reliable and dependable embedded systems has become increasingly important as the failure of these systems in an automotive, aerospace or nuclear application can have serious consequences.

Design and Test Technology for Dependable Systems-on-Chip covers aspects of system design and efficient modelling, and also introduces various fault models and fault mechanisms associated with digital circuits integrated into System on Chip (SoC), Multi-Processor System-on Chip (MPSoC) or Network on Chip (NoC). This book provides insight into refined "classical" design and test topics and solutions for IC test technology and fault-tolerant systems

Topics Covered:

- Built-in self repair for logic structures
- Combined test-data compression and test planning
- Diagnostic modeling of digital systems
- Fault simulation and fault injection technology
- Fault-tolerant and fail-safe design based on reconfiguration
- Flexible fault-tolerant schedules for embedded systems
- Memory testing and self-repair
- Optimizing fault tolerance for multi-processor system-on-chip
- Software-based self-test of embedded microprocessors
- Transient faults detection and compensation

Market: This premier publication is essential for all academic and research library reference collections. It is a crucial tool for academicians, researchers, and practitioners and is ideal for classroom use.

Raimund Ubar is a professor of computer engineering at Tallinn Technical University and the head of Centre of Excellence for Integrated Electronic Systems and Biomedical Engineering in Estonia. R. Ubar received his PhD degree in 1971 at the Bauman Technical University in Moscow. His main research interests include computer science, electronics design, digital test, diagnostics and fault-tolerance. He has published more than 250 papers and three books, lectured as a visiting professor in more than 25 universities in about 10 countries and served as a General Chairman for 10th European Test Conference, NORCHIP, BEC, EWDTC. He is a member of Estonian Academy of Sciences, Golden Core member of IEEE Computer Society and honorary professor of National University of Radioelectronics Charkiv (Ukraine). He was a chairman of Estonian Science Foundation and a member of the Academic Advisory Board of the Estonian President.